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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
08/903,453	07/29/1997	LEONARD FORBES	303.378US1	2271

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EXAMINER	
ECKERT II, GEORGE C	

ART UNIT	PAPER NUMBER
2815	

DATE MAILED: 12/21/2001

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 08/903,453	Applicant(s) Forbes et al.
	Examiner George C. Eckert II	Art Unit 2815

– The MAILING DATE of this communication appears on the cover sheet with the correspondence address –

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136 (a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) ☒ Responsive to communication(s) filed on *Sep 5, 2001*.

2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.

3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11; 453 O.G. 213.

Disposition of Claims

4) ☒ Claim(s) *2, 3, 24-28, 41-48, 50-52, and 65-68* is/are pending in the application.

4a) Of the above, claim(s) _____ is/are withdrawn from consideration.

5) ☐ Claim(s) _____ is/are allowed.

6) ☒ Claim(s) *2, 3, 24-28, 41-48, 50-52, and 65-68* is/are rejected.

7) ☐ Claim(s) _____ is/are objected to.

8) ☐ Claims _____ are subject to restriction and/or election requirement.

Application Papers

9) ☐ The specification is objected to by the Examiner.

10) ☐ The drawing(s) filed on _____ is/are objected to by the Examiner.

11) ☐ The proposed drawing correction filed on _____ is: a) ☐ approved b) ☐ disapproved.

12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. § 119

13) ☐ Acknowledgement is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d).

a) ☐ All b) ☐ Some* c) ☐ None of:

1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

*See the attached detailed Office action for a list of the certified copies not received.

14) ☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).

Attachment(s)

15) ☒ Notice of References Cited (PTO-892)

16) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

17) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s). *28*

18) ☐ Interview Summary (PTO-413) Paper No(s). _____

19) ☐ Notice of Informal Patent Application (PTO-152)

20) ☐ Other:

DETAILED ACTION

Request for Continued Examination

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on September 5, 2001 has been entered.

Response to Amendment

2. Applicant's amendment dated September 5, 2001 in which claims 1, 4-6, 20-23, 29-40, 49 and 53-64 were canceled has been entered of record.

Double Patenting

3. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970);and, *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321© may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

Claims 2 and 3 are provisionally rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 11-18 of co-pending Application No. 08/902,843. Although the conflicting claims are not identical, they are not patentably distinct from each other because the present invention and co-pending Application no. 08/902,843 disclose a transistor having:

a source and a drain separated by a channel supported by a semiconductor substrate;

a floating gate formed between the source and the drain above the channel and separated by an insulative amorphous carburized silicon layer;

a control gate formed adjacent to and insulated from the floating gate;

wherein the transistor is part of a memory cell comprising a capacitor.

Further, stacked capacitors are well known and widely used in memory devices.

This is a provisional obviousness-type double patenting rejection because the conflicting claims have not in fact been patented.

Claim Rejections - 35 U.S.C. § 103

The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

4. Claims 2, 3, 24-28, 41-48, 50-52 and 65-68 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sakata et al., *Amorphous silicon/amorphous silicon carbide heterojunctions*

applied to memory device structures, Electronics Letters, April 28, 1994, Vol. 30, No. 9 (of record), in view of JP 8-255878 to Sugita et al. (of record) and Burns et al., *Principles of Electronic Circuits.*

With regard to claims 2, 3, 24, 45, 46, 48, 50, 52, and 68, Sakata et al. teach in figure 1 the formation of an insulative layer of amorphous silicon carbide, shown as the a-SiC:H (graded) layer, formed on top of a substrate which is crystalline silicon (c-Si) that can be p-type (see *Sample Preparation*);

a floating gate formed of amorphous silicon, shown as the a-Si:H layer, formed above the amorphous silicon carbide insulator,

a second insulative layer of amorphous silicon carbide, shown as the a-SiC:H layer, formed above the a-Si:H floating gate, and

a control gate shown as metal in figure 1 and later taught as aluminum (see *Sample Preparation*).

And though Sakata et al. teach that the above structure "can be applied to floating-gate memory devices[,]" Sakata et al. do not teach the structure further comprising a source region, a drain region, or a channel region therebetween. However, such regions are taught by Sugita et al. Specifically, Sugita et al. teach, with reference to figure 1, a floating gate memory device comprising:

an N+ type source region 2 and an N+ type drain region 3 (see page 11, paragraph 0032 of the translated reference which states that the source and drains 2 and 3 are n+ type);

the source and drain regions formed in a p-type silicon substrate (see page 2 of the translated reference which lists the reference numerals and corresponding elements and shows that numeral 1 represents a p-type silicon substrate);

a channel region between the source and drain regions in the substrate (though the channel region is not numbered, it is inherent that there exists a channel region between the source and drain of a transistor, see *Principles of Electronic Circuits*, pp. 382-83 shows an n+ source and an n+ drain in a p-type substrate and refers to the device as one comprising an "n-channel");

a floating gate 6 (see page 3 of the translated reference and the list of elements which labels numeral 6 as a polysilicon floating gate) which is formed above and insulated from the substrate;

a control gate 8 formed above the floating gate and separated from the floating gate by a dielectric layer 7 (again, see the list of elements on page 3 of Sugita et al. where element 8 is labeled a control gate and element 7 is listed as SiO_2, a known, inherent insulator).

Sakata et al., Sugita et al. and Burns et al. are combinable because they are from the same field of endeavor, which field is the formation of floating gate devices. At the time of the invention it would have been obvious to a person of ordinary skill in the art to form a source region, drain region and channel region in the device of Sakata et al. The motivation for doing so is that the source, drain and channel regions allow individual floating gate devices to be formed in an array. That is, by forming source and drain regions having the floating gate stack therebetween, a plurality of floating gate devices can be formed in one substrate and yet be

individually written and erased by the use of the source, drain and channel regions. The use of the source/drain/channel regions for such programming is well known in the art. For example, Burns et al. explicitly teach such programming steps in the paragraph bridging pages 382-83. Furthermore, Sugita et al. generally teach this integration concept in paragraphs 0001 - 0005 of the translated reference. Therefore, it would have been obvious to combine Sakata et al with Sugita et al and Burns et al. to obtain the invention of claims 2, 3, 24-28, 41-48, 50-52 and 65-68.

Regarding the use of polysilicon as the material for the control gate, Sakata et al. indicate that the control gate is formed of aluminum while Sugita et al. are silent as to the material for their control gate. However, Burns et al. teach on page 382 that control gates (or, as there labeled, select gates) are typically formed of polysilicon. Even beyond the teaching of Burns et al., the use of polysilicon as a control gate is considered well known in the art. There are several advantages of using polysilicon as a control gate, for example, polysilicon can be doped to a low resistivity and is able to withstand higher temperatures so that it is unaffected during subsequent annealing steps. As such, it is considered obvious to form the control gate of Sakata et al. from polysilicon.

As to the method of formation of the insulation layer between the floating gate and the substrate from silicon carbide, Sakata et al. teach or in the alternative make obvious such a structure. The limitation that the amorphous carburized silicon is *grown* on the substrate is taught or in the alternative obvious over Sakata et al. In support of the process term *grown*, it is noted that applicant's *growth* method is a deposition (specification p. 6, lines 3-4). Sakata et al.

also teach a deposition method (see *Sample preparation*). As such, Sakata et al.'s deposition process anticipates the growth process limitation as instantly claimed.

In the alternative, and with further regard to the limitation where the *growth* process is further limited to be a microwave PECVD, limitations in the instant claims as to the process by which the final product is achieved do not distinguish over that taught by Sakata et al. That is, such limitations are product by process limitations. Note that a "product by process" claim or limitation is directed to the product per se, no matter how actually made, In re Hirao, 190 USPQ 15 at 17 (footnote 3). See also In re Brown, 173 USPQ 685; In re Luck, 177 USPQ 523; In re Fessmann, 180 USPQ 324; In re Avery, 186 USPQ 161; In re Wertheim, 191 USPQ 90 (209 USPQ 554 does not deal with this issue); In re Marosi et al, 218 USPQ 289; and particularly In re Thorpe, 227 USPQ 964, all of which make it clear that it is the patentability of the final product per se which must be determined in a "product by process" claim, and not the patentability of the process, and that an old or obvious product produced by a new method is not patentable as a product, whether claimed in "product by process" claims or not. Note that, once a product appearing to be substantially identical is found and a rejection is made, the burden shifts to the applicant to show an unobvious difference based on the claimed process steps. MPEP §2113. Instantly, because no evidence was proffered by applicant as to patentability based on the added process limitations, the burden remains with applicant to do so.

Response to Arguments

5. Applicant's arguments with respect to all claims have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to George C. Eckert II whose telephone number is (703) 305-2752.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mr. Eddie Lee can be reached on (703) 308-1690. The fax phone number for this Group is (703) 308-7722.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (703) 308-0956.

George C. Eckert II
Patent Examiner
Art Unit - 2815
November 19, 2001